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INFORMATION REPORT INFORMATION REPORT

CENTRAL INTELLIGENCE AGENCY

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C-O-N-F-I-D-E-N-T-I-A-LCOUNTRY **Rumania**REPORT

25X1

SUBJECT **Road Data**

DATE DISTR. 6 July 1959

NO. PAGES 1

REFERENCES

25X1

DATE OF INFO.

PLACE &

DATE ACQ.

25X1

THIS IS UNEVALUATED INFORMATION

25X1

1. A hard surface all weather road [#924] runs from Sighisoara south south-east to Brasov. The road has a good solid foundation and is over two lanes wide. It is considered to be a first class highway. The terrain through which this road runs is extremely hilly. The road can absorb heavy usage and is asphalt surfaced.
2. A loose surface, all weather road [#909] which is over one lane in width runs from Rupea west southwest to Lovnic where it veers and goes northward to Crit. The road is gravel surfaced and is able to absorb heavy usage.
3. A number of loose surface, dry weather dirt roads [935] run in the vicinity of Bunesti, Cobor, Lovnic and Dacia. The dirt roads are over one lane wide and occasionally are able to bear heavy usage. The dirt roads have a natural sand, gravel and rock subbase and foundation.
4. A number of cart tracks [#944] run in the same vicinity as the dirt weather roads [#935]. The cart tracks are approximately one lane in width and have a natural foundation of rock, gravel and sand. These cart tracks are occasionally capable of bearing heavy traffic.
5. The cart tracks are used by the villagers and farmers as short cuts to reach other roads, farms and are also used for inter-village communications.

25X1

C-O-N-F-I-D-E-N-T-I-A-L

STATE	ARMY	NAVY	AIR	FBI	AEC						
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INFORMATION REPORT INFORMATION REPORT

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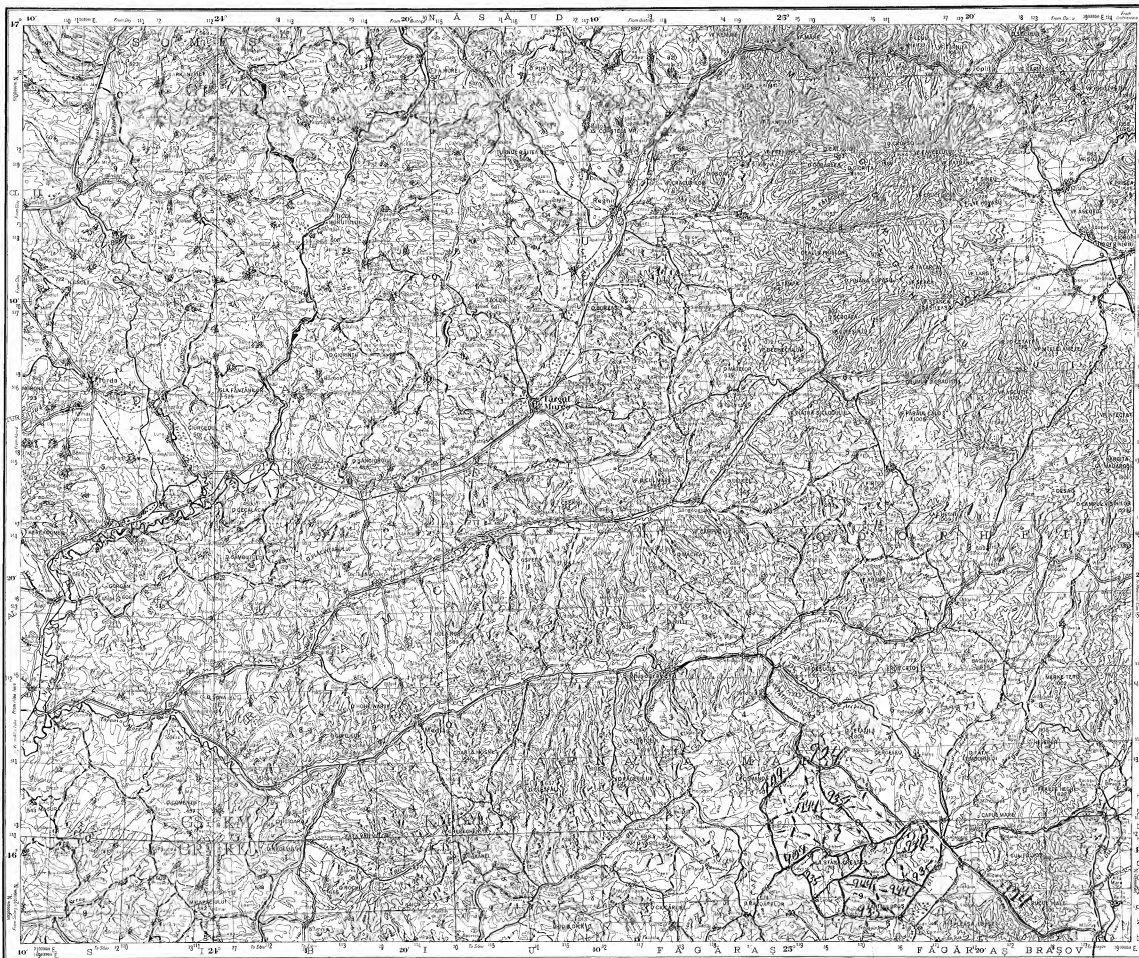
LIMITED

THE BALKANS 1 250,000

TÂRGUL MUREȘ,

EDITION 3-AMS

SHEET R-36
ANS SERIES W306



TRANSVERSE MERCATOR PROJECTION

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HEIGHTS IN METERS

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2	address	city	state

id	name	category	price	stock
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2	banana	fruit	0.8	200
3	orange	fruit	1.5	150
4	grape	fruit	2.0	80
5	pear	fruit	1.0	120
6	cherry	fruit	3.0	50
7	strawberry	fruit	4.0	30
8	kiwi	fruit	2.5	60
9	pineapple	fruit	5.0	20
10	mango	fruit	1.8	90
11	peach	fruit	1.4	110
12	plum	fruit	1.1	130
13	apricot	fruit	1.3	140
14	coconut	fruit	2.2	70
15	avocado	fruit	3.5	40
16	lemon	fruit	0.9	160
17	lime	fruit	0.7	180
18	citrus	fruit	1.6	100
19	watermelon	fruit	6.0	10
20	melon	fruit	4.5	15
21	honeydew	fruit	3.8	25
22	cantaloupe	fruit	3.2	35
23	jackfruit	fruit	7.0	5
24	guava	fruit	2.8	45
25	passion fruit	fruit	4.2	35
26	dragon fruit	fruit	5.5	20
27	lychee	fruit	3.0	40
28	rambutan	fruit	3.5	30
29	jackfruit	fruit	7.0	5
30	cashew	fruit	4.0	25
31	almond	fruit	5.0	15
32	walnut	fruit	6.0	10
33	pecan	fruit	7.0	5
34	hazelnut	fruit	8.0	5
35	macadamia	fruit	9.0	5
36	coconut	fruit	2.2	70
37	avocado	fruit	3.5	40
38	olive	fruit	1.0	120
39	fig	fruit	1.5	100
40	date	fruit	2.0	80
41	raisin	fruit	3.0	50
42	currant	fruit	4.0	30
43	elderberry	fruit	5.0	20
44	gooseberry	fruit	6.0	10
45	mulberry	fruit	7.0	5
46	blackberry	fruit	8.0	5
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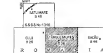
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COMPI LATION DIAGRAM



INDEX TO ADVERTISING SHEETS



<p>1. Problem Statement: Design a circuit that takes two 4-bit binary numbers as input and outputs their sum in 4-bit binary format.</p> <p>2. Inputs: Two 4-bit binary numbers, A and B.</p> <p>3. Outputs: A 4-bit binary sum, S.</p> <p>4. Constraints: The circuit must be implemented using only combinational logic gates (AND, OR, XOR, NOT).</p> <p>5. Assumptions: The inputs are valid 4-bit binary numbers.</p>	<p>1. Problem Statement: Design a circuit that takes two 4-bit binary numbers as input and outputs their sum in 4-bit binary format.</p> <p>2. Inputs: Two 4-bit binary numbers, A and B.</p> <p>3. Outputs: A 4-bit binary sum, S.</p> <p>4. Constraints: The circuit must be implemented using only combinational logic gates (AND, OR, XOR, NOT).</p> <p>5. Assumptions: The inputs are valid 4-bit binary numbers.</p>	<p>1. Problem Statement: Design a circuit that takes two 4-bit binary numbers as input and outputs their sum in 4-bit binary format.</p> <p>2. Inputs: Two 4-bit binary numbers, A and B.</p> <p>3. Outputs: A 4-bit binary sum, S.</p> <p>4. Constraints: The circuit must be implemented using only combinational logic gates (AND, OR, XOR, NOT).</p> <p>5. Assumptions: The inputs are valid 4-bit binary numbers.</p>	<p>1. Problem Statement: Design a circuit that takes two 4-bit binary numbers as input and outputs their sum in 4-bit binary format.</p> <p>2. Inputs: Two 4-bit binary numbers, A and B.</p> <p>3. Outputs: A 4-bit binary sum, S.</p> <p>4. Constraints: The circuit must be implemented using only combinational logic gates (AND, OR, XOR, NOT).</p> <p>5. Assumptions: The inputs are valid 4-bit binary numbers.</p>
<p>6. Design Approach: The circuit can be designed using a 4-bit ripple-carry adder. It consists of four full adders connected in series. The first full adder takes the least significant bits of A and B as input and produces the first bit of the sum (S₀) and a carry-out (C₁). Each subsequent full adder takes the next bits of A and B and the carry-in from the previous stage to produce the next bit of the sum (S₁, S₂, S₃) and the final carry-out (C₄).</p> <p>7. Logic Diagram: The logic diagram shows the internal structure of the 4-bit ripple-carry adder. It uses four full adders, each implemented with two 3-input OR gates, two 3-input AND gates, and one 3-input XOR gate. The carry-in (C₀) is set to 0, and the carry-out (C₄) is the final carry-out of the circuit.</p>	<p>6. Design Approach: The circuit can be designed using a 4-bit ripple-carry adder. It consists of four full adders connected in series. The first full adder takes the least significant bits of A and B as input and produces the first bit of the sum (S₀) and a carry-out (C₁). Each subsequent full adder takes the next bits of A and B and the carry-in from the previous stage to produce the next bit of the sum (S₁, S₂, S₃) and the final carry-out (C₄).</p> <p>7. Logic Diagram: The logic diagram shows the internal structure of the 4-bit ripple-carry adder. It uses four full adders, each implemented with two 3-input OR gates, two 3-input AND gates, and one 3-input XOR gate. The carry-in (C₀) is set to 0, and the carry-out (C₄) is the final carry-out of the circuit.</p>	<p>6. Design Approach: The circuit can be designed using a 4-bit ripple-carry adder. It consists of four full adders connected in series. The first full adder takes the least significant bits of A and B as input and produces the first bit of the sum (S₀) and a carry-out (C₁). Each subsequent full adder takes the next bits of A and B and the carry-in from the previous stage to produce the next bit of the sum (S₁, S₂, S₃) and the final carry-out (C₄).</p> <p>7. Logic Diagram: The logic diagram shows the internal structure of the 4-bit ripple-carry adder. It uses four full adders, each implemented with two 3-input OR gates, two 3-input AND gates, and one 3-input XOR gate. The carry-in (C₀) is set to 0, and the carry-out (C₄) is the final carry-out of the circuit.</p>	<p>6. Design Approach: The circuit can be designed using a 4-bit ripple-carry adder. It consists of four full adders connected in series. The first full adder takes the least significant bits of A and B as input and produces the first bit of the sum (S₀) and a carry-out (C₁). Each subsequent full adder takes the next bits of A and B and the carry-in from the previous stage to produce the next bit of the sum (S₁, S₂, S₃) and the final carry-out (C₄).</p> <p>7. Logic Diagram: The logic diagram shows the internal structure of the 4-bit ripple-carry adder. It uses four full adders, each implemented with two 3-input OR gates, two 3-input AND gates, and one 3-input XOR gate. The carry-in (C₀) is set to 0, and the carry-out (C₄) is the final carry-out of the circuit.</p>
<p>8. Implementation: The circuit was implemented using a logic simulator. The inputs A and B were set to 1011 and 1010, respectively. The output S was 0110, which is the correct sum of 1011 and 1010.</p> <p>9. Conclusion: The 4-bit ripple-carry adder circuit successfully implements the addition of two 4-bit binary numbers. The circuit is simple and easy to implement using basic logic gates.</p>	<p>8. Implementation: The circuit was implemented using a logic simulator. The inputs A and B were set to 1011 and 1010, respectively. The output S was 0110, which is the correct sum of 1011 and 1010.</p> <p>9. Conclusion: The 4-bit ripple-carry adder circuit successfully implements the addition of two 4-bit binary numbers. The circuit is simple and easy to implement using basic logic gates.</p>	<p>8. Implementation: The circuit was implemented using a logic simulator. The inputs A and B were set to 1011 and 1010, respectively. The output S was 0110, which is the correct sum of 1011 and 1010.</p> <p>9. Conclusion: The 4-bit ripple-carry adder circuit successfully implements the addition of two 4-bit binary numbers. The circuit is simple and easy to implement using basic logic gates.</p>	<p>8. Implementation: The circuit was implemented using a logic simulator. The inputs A and B were set to 1011 and 1010, respectively. The output S was 0110, which is the correct sum of 1011 and 1010.</p> <p>9. Conclusion: The 4-bit ripple-carry adder circuit successfully implements the addition of two 4-bit binary numbers. The circuit is simple and easy to implement using basic logic gates.</p>